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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/080,036 | 02/19/2002 | Vani Verma | 5732-00300 | 3980 |

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| EXAMINER |
|---|
| THAI, LUAN C |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/080,036 | VERMA ET AL. | |
| | Examiner | Art Unit | |
| | Luan Thai | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14,15,17,19 and 20* is/are rejected.

7)☒ Claim(s) *12,13,16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election *without traverse* of Embodiment II, set forth in Figure 7, claims 1-20, in Paper No. 6 is acknowledged. Claim 1 is generic.

2. Claims 21-31 have been canceled (paper No. 6).

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaoka et al. (6,583,512) in view of Corisis et al. (6,515,359).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-7, Nakaoka et al. disclose a memory module comprising: a plurality of conductors (32), each of which has opposed first and second ends; a stacked pair of ICs coupled to the first end of each of the conductors by the first set of wires (34) extending from the bonding pads (12) of the first IC (10); a molded resin (35) encasing the stacked ICs and having an outer surface on which the second end of each conductors (32) terminated near the edges of the memory module; the bonding pads (11) of the first IC (10) coupled to the bonding pads (21) of the second IC (20); wherein the lower surface

of the first IC (10) is bonded to an upper surface of a conductive plate (31) and the lower surface of the conductive plate (31) extends flush with the outer dimension of the stacked ICs. Nakaoka et al fail to teach the conductors terminating in a single row near an edge of the module.

Corisis et al. while related to a similar memory chip package design teach the lead frame (102) having a plurality of conductor leads (104-105) terminating in a single row near an edge of the module for external connection, wherein a first set of wires (124) connected between the bonding pads (120) of the IC (100) and a second set of wires (124) transmitted ground signals between the bonding pads (120) of the IC (100) and the conductors (114/112). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakaoka et al's memory module by apply the lead frame having conductors terminating in a single row near an edge of the module, as taught by Corisis et al., in order to make the package to be capable mounted vertically on a mother board.

5. Claims 8-11, 14-15, 17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaoka et al. (6,583,512) and Corisis et al. (6,515,359), as applied for claim 1, and further in view of Nishizawa et al (6,531,773).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 8-11, 14-15, 17 and 19-20, the proposed device of Nakaoka et al. and Corisis et al. discloses all the limitations of the claimed invention as detailed above except for specifying the pair of ICs comprising storage elements and a controller.

A pair of stacked memory ICs comprising storage elements and a controller, however, is conventional in semiconductor art, as taught by Nishizawa et al (see figures 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the proposed device of Nakaoka et al. and Corisis et al. with the pair of ICs comprising storage elements and a controller, as taught by Nishizawa et al, since such structure is conventional in semiconductor art, specifically in memory module art.

***Allowable Subject Matter***

6. Claims 12-13, 16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken either singly or in combination fails to anticipate or fairly suggest: a) *an outer edge of the memory module being adapted for slideable engagement into a receptor that is electrically connected to an electronic system*, as recited in claim 12; b) a ring coplanar with and laterally from the ground element, as recited in claim 16; c) the memory module being mechanically and electrically interchangeable with a memory card, and wherein the entire outer dimension of the module except for the second end of the conductors is surrounded by a covering that employs a mechanical tab which, when actuated, prevents writing data to the integrated circuits, as recited in claim 18; especially when these limitations are considered within the specific combination claimed.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
June 30, 2003